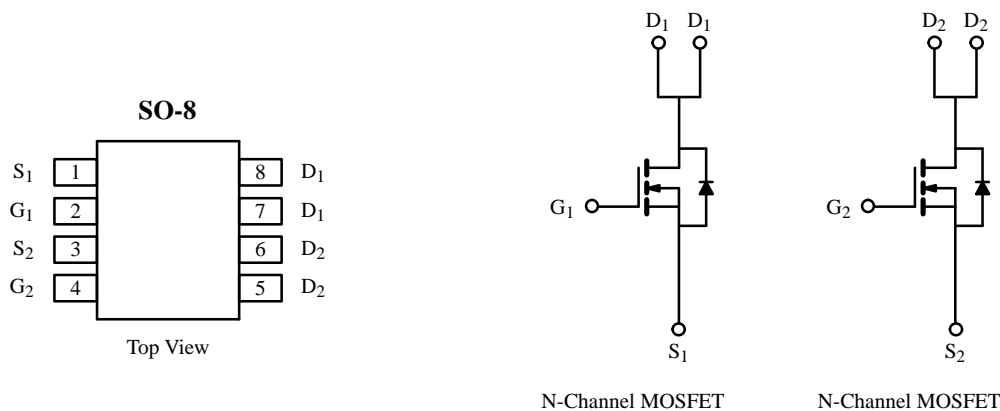


Dual N-Channel Enhancement-Mode MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
50	0.13 @ V _{GS} = 10 V	± 3.0
	0.20 @ V _{GS} = 4.5 V	± 1.5

Recommended upgrade: Si9945DY



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	50	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	± 3.0
		T _A = 70°C	± 2.3
Pulsed Drain Current	I _{DM}	± 10	A
Continuous Source Current (Diode Conduction) ^a	I _S	2.0	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	2.0
		T _A = 70°C	1.3
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1221. A SPICE Model data sheet is available for this product (FaxBack document #5113).

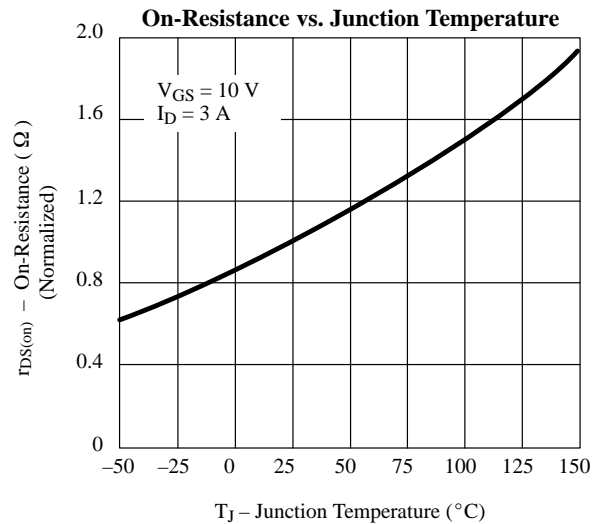
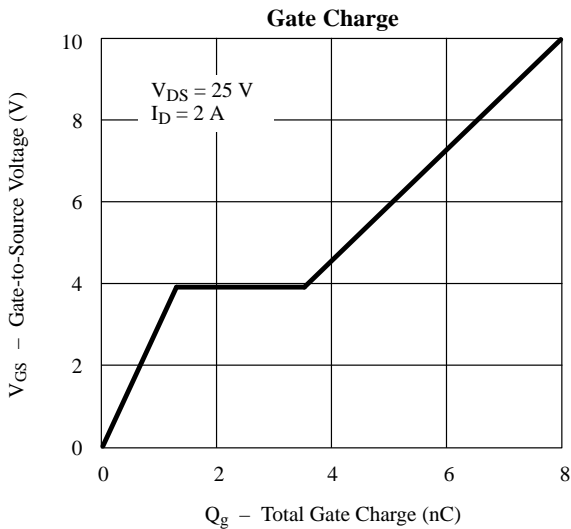
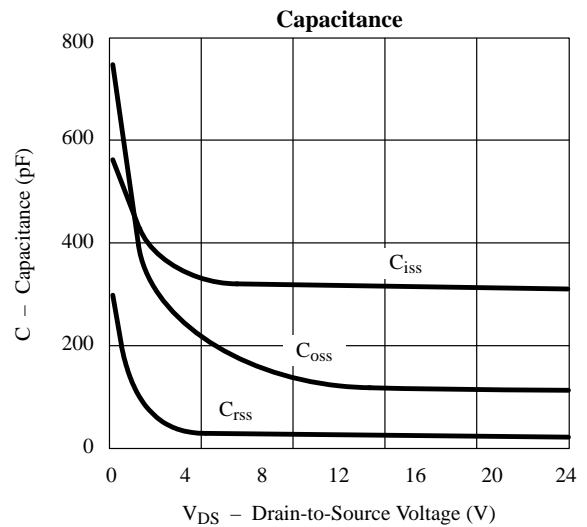
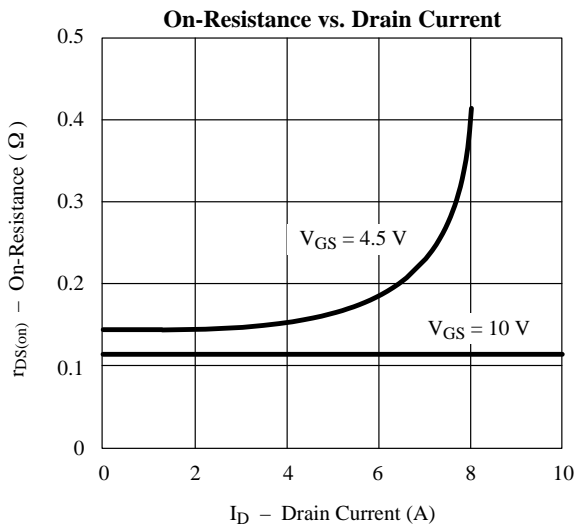
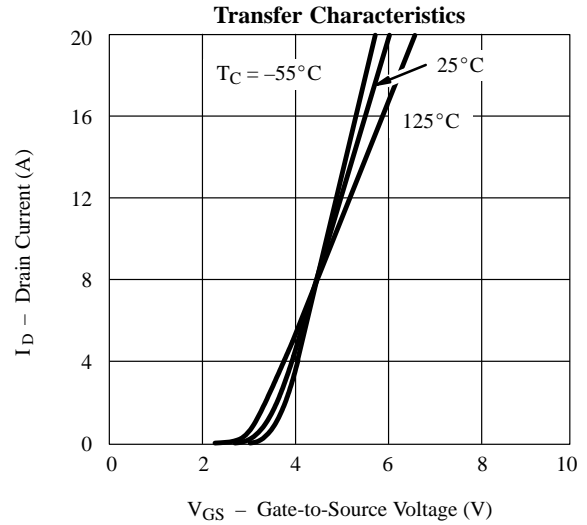
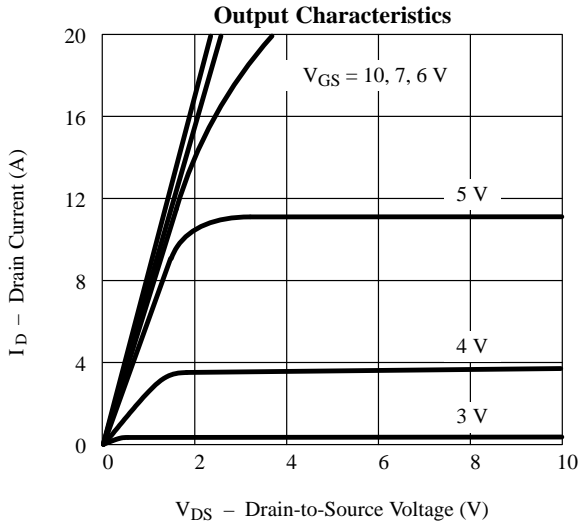
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$			2	μA
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			25	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	10			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 3.0 \text{ A}$		0.11	0.13	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 1.5 \text{ A}$		0.15	0.20	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 3.0 \text{ A}$		5.5		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 25 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$		8.0	30	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			2.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 \text{ V}, R_L = 25 \Omega$ $I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		9	20	ns
Rise Time	t_r			8	20	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			25	50	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		70	100	

Notes

- Guaranteed by design, not subject to production testing.
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

